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**1 System simulation of printed circuit boards including packages and connectors**   
 K. Adamiak, R. Allen, J. Poltz, C. Rebizant, A. Wexler  
 January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**  
**Publisher:** ACM Press  
 Full text available:  pdf(573.59 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)  
 An efficient method for analog simulation of printed circuit board systems is proposed. It is based on the transmission line model derived from the analysis of the electromagnetic field in a two-dimensional cross-section of devices. Simulation results for two circuits with IC package, cable and connector models are presented. The results confirm the effectiveness of this method.

**2 A new time-domain macromodel for transient simulation of uniform/nonuniform multiconductor transmission-line interconnections**   
 Monjurul Haque, Ali El-Zein, S. Chowdhury  
 June 1994 **Proceedings of the 31st annual conference on Design automation**  
**Publisher:** ACM Press  
 Full text available:  pdf(119.29 KB) Additional Information: [full citation](#), [references](#), [index terms](#)

**3 Efficient transient simulation of lossy interconnect**   
 Jaijeet S. Roychowdhury, Donald O. Pederson  
 June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**  
**Publisher:** ACM Press  
 Full text available:  pdf(639.45 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

**4 A general dispersive multiconductor transmission line model for interconnect simulation in SPICE**   
 Mustafa Celik, Andreas C. Cangellaris  
 January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**  
**Publisher:** IEEE Computer Society  
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Although numerous methods have been proposed for interconnect simulation, no single model exists for all kind of transmission line problems. This paper presents a new, single, general dispersive coupled uniform/nonuniform transmission line model which can be used for interconnect simulation in SPICE. The mathematical model is based on the use of Chebyshev polynomials for the representation of the spatial variation of the transmission-line voltages and currents. A simple collocation procedure is ...

**Keywords:** transient analysis, multiconductor transmission lines, interconnect simulation, Chebyshev approximation

**5** [Fast parameters extraction of general three-dimension interconnects using geometry](#)

[independent measured equation of invariance](#)

Weikai Sun, Wayne Wei-Ming Dai, Wei Hong

June 1996 **Proceedings of the 33rd annual conference on Design automation**

**Publisher:** ACM Press

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**6** [Transient simulation of lossy coupled transmission lines](#)

Shen Lin, Ernest S. Kuh

November 1992 **Proceedings of the conference on European design automation**

**Publisher:** IEEE Computer Society Press

Full text available: [pdf\(550.45 KB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)

**7** [On-chip inductance issues in multiconductor systems](#)

Shannon V. Morton

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

**Publisher:** ACM Press

Full text available: [pdf\(136.17 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

**Keywords:** RLC, alpha microprocessor, buses, capacitance, cross-talk, inductance, interconnect, noise, resistance, semiconductor, transmission line

**8** [A novel dimension reduction technique for the capacitance extraction of 3D VLSI interconnects](#)

Wei Hong, Weikai Sun, Zhenhai Zhu, Hao Ji, Ben Song, Wayne Wei-Ming Dai

January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

**Publisher:** IEEE Computer Society

Full text available: [pdf\(178.91 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

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In this paper, we present a new capacitance extraction method named Dimension Reduction Technique (DRT) for 3D VLSI interconnects. The DRT converts a complex 3D problem into a series of cascading simple 2D problems. Each 3D problem is solved separately, so we can choose the most efficient method according to the arrangement of conductors. More importantly, it is very easy to obtain the analytical solutions of 2D

problem in many layers such as the pure dielectric layers and the layers with parallel ...

**Keywords:** 3D VLSI interconnects, DRT, Dimension Reduction Technique, FastCap, SPICELINK, VLSI, capacitance extraction, dielectric layers, parallel signal lines

**9 An Ethernet compatible low cost/high performance communication solution**

◆ I. Chlamtac, A. Herman

August 1987 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM workshop on Frontiers in computer communications technology SIGCOMM '87**, Volume 17 Issue 5

**Publisher:** ACM Press

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The LAN-HUB is a new local area network designed to combine the properties of several existing LAN standards to provide highly reliable communication at a relatively lower cost per station, improve network capacity/delay performance and increase the LAN user's flexibility in configuring his network. The LAN-HUB network is configured around the CODEX 4320 LAN-HUB communication controllers which allow up to eight Ethernet/IEEE 802.3 stations to transparently share one network transceiver or R ...

**10 Dynamic algorithm transformation (DAT) for low-power adaptive signal processing**

◆ Manish Goel, Naresh R. Shanbhag

August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**

**Publisher:** ACM Press

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**11 Layout analysis: Electrical modelling of lossy on-chip multilevel interconnecting lines**

K. Z. Dimopoulos, J. N. Avaritsiotis, S. J. White

February 1991 **Proceedings of the conference on European design automation**

**Publisher:** IEEE Computer Society Press

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A self contained method for the electrical modelling of lossy 3-D multilevel interconnections has been developed. The method allows for the generation of a multiple coupled line model, compatible with SPICE-like CAD programs, from the interconnection line constants and parasitic coupling parameters which are computed by the so-called method of moments. The proposed method can be used for the analysis of coupled line systems with linear or nonlinear/time varying terminators, as well as for the st ...

**12 Deterministic service guarantees in IEEE 802.12 networks—part I: the single-hub case**

Peter Kim

October 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 5

**Publisher:** IEEE Press

Full text available:  pdf(357.99 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

**Keywords:** IEEE 802.12, guaranteed service, local area network, resource reservation

**13 TRICAP—a three dimensional capacitance solver for arbitrarily shaped conductors**

on printed circuit boards and VLSI interconnections

Matthias Tröscher, Hans Hartmann, Georg Klein, Andreas Plettner

September 1994 **Proceedings of the conference on European design automation****Publisher:** IEEE Computer Society PressFull text available:  pdf(524.51 KB) Additional Information: [full citation](#), [references](#), [index terms](#)**14 Passive Synthesis of Compact Frequency-Dependent Interconnect Models via Quadrature Spectral Rules**

Traianos Yioultsis, Anne Woo, Andreas C. Cangellaris

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design****Publisher:** IEEE Computer SocietyFull text available:  pdf(245.88 KB) Additional Information: [full citation](#), [abstract](#), [index terms](#)

In this paper, we present a reduced order modeling methodology, based on the utilization of optimal non-uniform grids generated by Gaussian spectral rules, for the direct passive synthesis of SPICE-compatible modeling of multi-conductor interconnect structures. The algorithm is based on a Padé-Chebyshev approximation of the frequency-dependent input impedance matrix of the passive interconnect system. The synthesized circuit is represented as the concatenation of a number of non-uniform sections of pass ...

**Keywords:** Transmission-line modeling of interconnects, interconnects with frequency-dependent losses, passive reduced-order synthesis

**15 Efficient simulation of lossy and dispersive transmission lines**

Tuyen V. Nguyen

June 1994 **Proceedings of the 31st annual conference on Design automation****Publisher:** ACM PressFull text available:  pdf(166.29 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)**16 Twenet: A LAN with message priorities, design and performance considerations.**

I. G. Niemegeers, C. A. Vissers

June 1984 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM SIGCOMM symposium on Communications architectures and protocols: tutorials & symposium SIGCOMM '84**, Volume 14 Issue 2**Publisher:** ACM PressFull text available:  pdf(731.45 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper discusses design and performance aspects of Twenet, one of the few implemented LANs which offers a service based on message priorities. The medium access mechanism uses the CSMA/CD principle, however with a deterministic collision resolution method. These characteristics make Twenet suitable for real-time applications, as well as a mixture of real-time and non real-time applications. The general system structure is introduced followed by a detailed description of the priori ...

**17 Performance modelling of the Orwell basic access mechanism**

M. Zafirovic, I. G. Niemegeers

August 1987 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM workshop on Frontiers in computer communications technology SIGCOMM '87**, Volume 17 Issue 5**Publisher:** ACM Press

Full text available:  pdf(1.03 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Orwell is a high speed slotted ring. Its protocol uses destination release of the slots. Because of this the carried load can be much larger than the transmission rate. A new analytical model of the Orwell basic access mechanism is presented in this paper. The model shows to be accurate and usable over a wide range of parameters. The performance analysis of the Orwell basic access mechanism is presented.

18 [Efficient and passive modeling of transmission lines by using differential quadrature method](#) 

Q. Xu, P. Mazumder

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Press

Full text available:  pdf(171.50 KB) Additional Information: [full citation](#), [references](#), [index terms](#)

19 [Time domain analysis of nonuniform frequency dependent high-speed interconnects](#) 

Sanjay L. Manney, Michel S. Nakhla, Qi-jun Zhang

November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society Press

Full text available:  pdf(474.68 KB) Additional Information: [full citation](#), [references](#), [index terms](#)

20 [A sparse image method for BEM capacitance extraction](#) 

 Byron Krauter, Yu Xia, Aykut Dengi, Lawrence T. Pileggi

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Publisher: ACM Press

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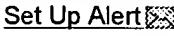
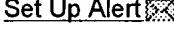
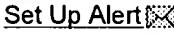
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5	BRS	L5	28	(hardware same emulat\$4) and ((circuit adj boards) same plurality same printed) and (integrated adj circuits) and (emulation same logic same design)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:13

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7	BRS	L7	28	(hardware same emulat\$4) and ((circuit adj boards) same plurality same printed) and (integrated adj circuits) and (emulation same logic same design)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:14
8	BRS	L8	3109	(multiconductor adj cable)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:17
9	BRS	L9	1041	(multiconductor adj cable) and (inputs same outputs)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:17
10	BRS	L10	34	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:18

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12	BRS	L12	0	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length)) and (test near pattern)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:19
13	BRS	L13	0	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length)) and (test adj pattern)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:19
14	BRS	L14	34	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:20
15	BRS	L15	0	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length)) and (integrated adj circuit adj boards)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:20

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	3	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length)) and (integrated adj circuit)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 13:03
17	BRS	L17	2	(test adj pattern) same (cable adj length)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:25
18	BRS	L18	0	((test adj pattern) same (cable adj length)) and multi-conductor	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:25
19	BRS	L19	0	(multiconductor adj cable) same emulation same length	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 13:03
20	BRS	L20	2	((multiconductor adj cable) same emulation) and length	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 13:03

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21	BRS	L21	7	((multiconductor adj cable) and emulation) and length	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 13:04
22	BRS	L22	2	((multiconductor adj cable) same emulation) and length	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 13:31
23	BRS	L23	12	(prior adj installing adj cable)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 13:31
24	BRS	L24	0	(prior adj installing adj cable) and (interchanging same inputs same outputs)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 13:32
25	BRS	L25	0	(prior adj installing adj cable) and (interchang\$4)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 13:32

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27	BRS	L27	166	(determin\$4 adj cable adj length)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 14:03
28	BRS	L28	276	(multiconductor same interconnected)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 14:04
29	BRS	L29	223	(multiconductor same interconnected same cable)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 14:04
30	BRS	L30	18	(multiconductor same interconnected same cable) and (determine same length)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 14:05

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31	BRS	L31	0	(multiconductor same interconnected same cable) and (determine adj length)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 14:05
32	BRS	L32	18	(multiconductor same interconnected same cable) and (determine same length)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 14:05

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11	BRS	L11	1	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length)) and (test same pattern)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:18
12	BRS	L12	0	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length)) and (test near pattern)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:19
13	BRS	L13	0	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length)) and (test adj pattern)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:19
14	BRS	L14	34	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:20
15	BRS	L15	0	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length)) and (integrated adj circuit adj boards)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:20

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	3	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length)) and (integrated adj circuit)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:23
17	BRS	L17	2	(test adj pattern) same (cable adj length)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:25
18	BRS	L18	0	((test adj pattern) same (cable adj length)) and multi-conductor	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:25

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	164	(hardware same emulat\$4) and ((circuit adj boards) same plurality)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:12
2	BRS	L2	103	(hardware same emulat\$4) and ((circuit adj boards) same plurality same printed)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:12
3	BRS	L3	67	(hardware same emulat\$4) and ((circuit adj boards) same plurality same printed) and (integrated adj circuits)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:13
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5	BRS	L5	28	(hardware same emulat\$4) and ((circuit adj boards) same plurality same printed) and (integrated adj circuits) and (emulation same logic same design)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:13

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6	BRS	L6	0	(hardware same emulat\$4) and ((circuit adj boards) same plurality same printed) and (integrated adj circuits) and (emulation same logic same design) and (multiconductor adj cable)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:17
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8	BRS	L8	3109	(multiconductor adj cable)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:17
9	BRS	L9	1041	(multiconductor adj cable) and (inputs same outputs)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:17
10	BRS	L10	34	(multiconductor adj cable) and (inputs same outputs) and (determin\$3 same (cable adj length))	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 12:18

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3	BRS	L4	1639	716/5.ccls.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/04/25 16:40